

# EENG 2710 Digital Logic Design

## Fall 2016

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**Instructor:** Dr. Murali Varanasi

**Room:** NTDP B 242

**Time:** TR 8:30 a.m. - 9:50 a.m.

**Office:** Discovery Park B-263

**Office hours:** MT 10 a.m. - Noon or by appointment

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**Office:** Discovery Park B-251

**Office Hours:** MW 11 a.m. – 1 p.m. or by appointment

### **Textbook(s) and/or required material:**

*Digital Logic Circuit Analysis & Design*, Victor P. Nelson, H. Troy Nagle, J. David Irwin, Bill D. Carroll, ISBN-10: 0134638948, Prentice Hall, 1995.

### **Course Objectives (Courtesy of Dr. Gayatri Mehta)**

The main objectives of the course are to facilitate the students to achieve the highest levels in the Bloom's 6-level Learning Taxonomy so that they, at the end of the course, will be able to-

1. **Know** *what* the digital systems are, *how* they differ from analog systems and *why* it is advantageous to use the digital systems in *many applications*.
2. **Comprehend** different number systems including the binary system and Boolean algebraic principles
3. **Apply** Boolean algebra to switching logic design and simplification.
4. **Analyze** a given digital system and decompose it into logical blocks involving both *combinational* and *sequential circuit* elements.
5. **Synthesize** a given system starting with problem requirements, identifying and designing the building blocks, and then integrating blocks designed earlier
6. **Validate** the system functionality and evaluate the relative merits of different designs.

### **Course Learning Outcomes (CLOs)**

Course Learning Outcomes (CLOs), that is, the areas for student learning in this course are:

- [CLO-1]** Digital and Analog Systems: Basic Concepts and Historical Perspective  
Importance of Learning to Learn (L2L) and Project-Based Learning (PBL) in learning Digital Logic Design.
- [CLO-2]** Number Systems and Digital Logic Gates
- [CLO-3]** Boolean Algebra, Switching Functions and Canonical Forms
- [CLO-4]** Combinational Circuit Minimization, Analysis, and Synthesis
- [CLO-5]** Sequential circuits elements and sequential logic circuits
- [CLO-6]** Modular Sequential Logic- Counters and shift registers

<b>[CLO-7]</b>	Minimization of Synchronous Sequential Circuits
<b>[CLO-8]</b>	Analysis and Design of asynchronous sequential circuits
<b>[CLO-9]</b>	Digital Logic Testing
<b>[CLO-10]</b>	Digital Project execution from requirements through design and testing
<b>[CLO-11]</b>	Professional presentation of assignments and project reports

**Course Outline and Tentative Schedule:**

<b>Topic No.</b>	<b>Topics</b>
1.	Digital and analog systems- an introduction, historical perspective, importance of L2L and PBL
2.	Number systems and codes
3.	Boolean Algebra, Switching functions and canonical forms
4.	Circuit minimization, Analysis of combinational circuits, and Timing issues
5.	Top-down Modular Design of Combinational Logic
6.	Sequential Circuit Elements- Latches and flip-flops
7.	Modular Sequential Logic- Counters and shift registers
8.	Analysis and Design of synchronous sequential circuits
9.	Analysis and Design of asynchronous sequential circuits
10.	Digital Logic Testing

**Exams:** There will be three exams including the final exam.

**Missed Exams:**

You will be allowed to make up a missed exam **if and only if** you have a documented university excused absence and received **prior** approval from the instructor.

**Assignments:** No late assignments will be accepted.

**Attendance Policy:**

In view of the continuous evaluation strategy adopted by the instructor, perfect attendance is recommended for those aspiring to get good grades. Rather than taking attendance, there will be pop quizzes. A quiz may be administered at the beginning, middle, or end of a class session.

**Grading:**

- Assignments: 10%
- Exam 1: 25%
- Exam 2: 25%
- Final: 35%
- Project: 5%

**Academic Dishonesty:**

Cheating will not be tolerated. Anyone found guilty of cheating on a test or assignment will be awarded an F grade for the course. Discussions of problems and assignment with your classmates is welcome and

encouraged, however, sharing of solutions is not. If you need help, you should ask the instructor. Cheating includes, but is not limited to, all forms of plagiarism and misrepresentation. For your rights and responsibilities please refer to <http://www.unt.edu/csrr>

### **Disabilities Accommodation:**

The University of North Texas complies with Section 504 of the 1973 Rehabilitation Act and with the Americans with Disabilities Act of 1990. The University of North Texas provides academic adjustments and auxiliary aids to individuals with disabilities, as defined under the law. Among other things, this legislation requires that all students with disabilities be guaranteed a learning environment that provides for reasonable accommodation of their disabilities. If you believe you have a disability requiring accommodation, please see the instructor and/or contact the Office of Disability Accommodation at 940-565-4323 during the first week of class.

### **Additional Policies and Procedures:**

Cell Phones: Please remember to turn off phones prior to class.

Extra Help: PLEASE DO NOT WAIT UNTIL THE LAST MINUTE. If you are having trouble with this class, please come by my office during office hours. I am also available by e-mail at [Murali.Varanasi@unt.edu](mailto:Murali.Varanasi@unt.edu)

### **Reading Requirements:**

The students are required to come prepared to every class with the material discussed in the previous class.

### **Our EE Program Outcomes (POs)**

Upon completion of our BSEE program, the students will be able to:

**[PO-1]** Apply knowledge of mathematics, engineering and science.

**[PO-2]** Design and conduct experiments to verify and validate the design projects developed by them, and analyze and interpret data.

**[PO-3]** Develop project-based learning skills through design and implementation of a system, component, or process that meets the needs within realistic constraints.

**[PO-4]** Function on multidisciplinary teams.

**[PO-5]** Identify, formulate, and solve engineering problems.

**[PO-6]** Have an understanding of professional and ethical responsibility.

**[PO-7]** Communicate effectively.

**[PO-8]** Achieve broad education necessary to understand the impact of electrical engineering solutions in a global and societal context.

**[PO-9]** Understand learning processes, concepts of learning to learn, and engage in lifelong learning.

**[PO-10]** Achieve knowledge of contemporary issues.

**[PO-11]** Use techniques, skills, and computer-based tools for conducting experiments and carrying out designs.

**[PO-12]** Develop an appreciation for principles of business practices and entrepreneurship.

**ABET Outcomes**

**3a-** an ability to apply knowledge of mathematics, science, and engineering

**3b-** an ability to design and conduct experiments, as well as to analyze and interpret data

**3c-** an ability to design a system, component, or process to meet desired needs

**3d-** an ability to function on multi-disciplinary teams

**3e-** an ability to identify, formulate, and solve engineering problems

**3f-** an understanding of professional and ethical responsibility

**3g-** an ability to communicate effectively

**3h-** the broad education necessary to understand the impact of engineering solutions in a global and societal context

**3i-** a recognition of the need for, and an ability to engage in life-long learning

**3j-** a knowledge of contemporary issues

**3k-** an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice

**Relationship between the Course Learning Outcomes and Program/ABET Outcomes**

The course learning outcomes map onto the program and ABET outcomes as depicted in the table below.

CLO	Program Outcomes/ABET Outcomes											
	PO-1/ 3(a)	PO-2/ 3(b)	PO-3/ 3(c)	PO-4/ 3(d)	PO-5/ 3(e)	PO-6/ 3(f)	PO-7/ 3(g)	PO-8/ 3(h)	PO-9/ 3(i)	PO-10/ 3(j)	PO-11/ 3(k)	PO-12
1								x				
2									x			
3	x											
4	x											
5	x											
6	x											
7	x											
8	x											
9	x											
10	x	x										
11		x	x				x				x	